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- [2] H. Alexanian et al; "Optimized digital feature extraction in the FERMI microsystem", NIM A 357 (1995) pp 318-328
- [3] CMS Calorimeter Trigger Group; "CMS Calorimeter Trigger, Preliminary Specifications of the Baseline Trigger Algorithms" CMS TN/96-10
- [4] S. Cittolin et al; "Front End Logical Model in CMS", CMS TN/96-015

The MCM has been developed within the EUROPRACTICE programme thus allowing access to multiple industries for the production. The MCMs will be delivered tested and guaranteed by industry.

11.5.2 Readout VME module

A Readout Module, built as a 9U VME module, contains 15 MCMs and associated functions like Board Controller and interface to the DDU and trigger. This gives 60 channels or 30 trigger towers per module. The Board Controller will be in the form of a FPGA or EPLD. Estimated power dissipation is around 50 W per module.

The Readout Module will be produced by industry and delivered tested and guaranteed. A total of 250 modules are needed to read out the HCAL detector

11.5.3 Crate system

The type of crate to be used will be the standard CMS 9U VME crates.

Each crate houses 18 Readout Modules, the DDU/FED module and a Local Control module or an interface to a shared Local Controller. A custom backplane is used for the Data path connections inside the crate and the Transition module at the back of the crate will be used for the optical connections and interfacing.

A total of 14 crates are foreseen for the total system which corresponds to the data volume requirement of 14 RDPMs.

11.5.4 Quality control, assurance, and monitoring

The totality of the items will be produced by industry and a ISO 9000 compatible follow-up process will be used. This guarantees the best possible quality control, assurance and monitoring during the total production chain. All items will carry at least a 1 year guarantee by the manufacturer which should be followed by maintenance contract to be renegotiated at regular intervals.

11.6 ACCESS AND MAINTENANCE

11.6.1 Access

All electronics, except the on-detector front-end part, is placed in the counting room and therefore, is continuously accessible.

11.6.2 Maintenance

As stated in chapter 11.5.4 all items will be covered by an initial guarantee period followed by set of maintenance contracts. A set of spare items, around 10%, will be made available.

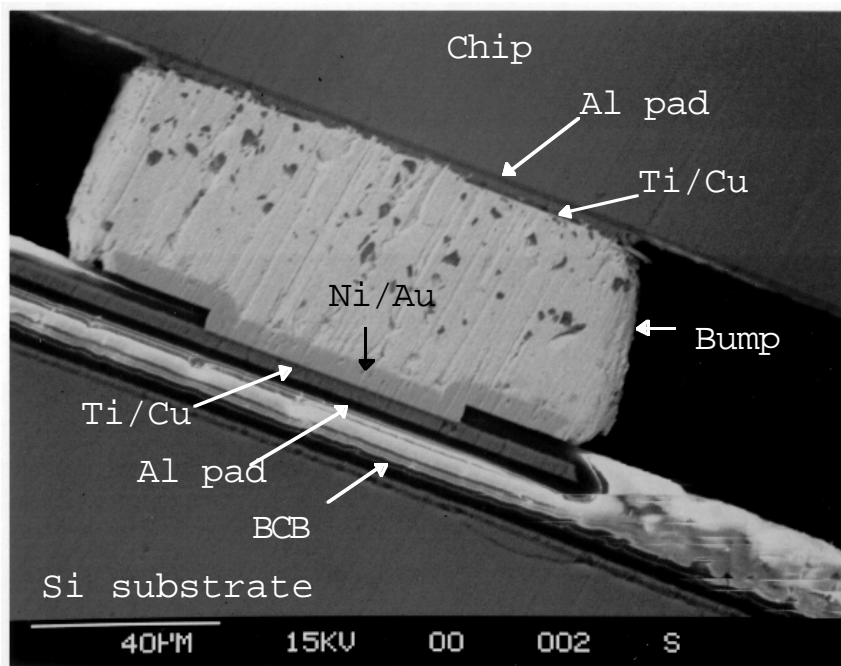


Fig. 11.20: Scanning electron microscope cross-section of a flip-chip mounted die.

The HCAL MCM contains a set of the above described ASICs capable of processing four channels and to generate two trigger tower information including the trigger primitives pipelines. The goal is to get the dimensions of the MCM down to less than 45 x 45 mm by migrating the existing ASICs, now in 0.8 μm and 0.7 μm technology, to a high-performance deep sub-micron technology, e.g. 0.5 μm or better with three metal layers. This is possible as the environment in the counting room allow the use of classical CMOS technologies i.e. no radiation problems.

Fig. 11.21 shows a prototype MCM system produced by the RD16-FERMI project which was used to evaluate the reliability of the technology. Extensive temperature cycling have been done without any sign of fatigue.

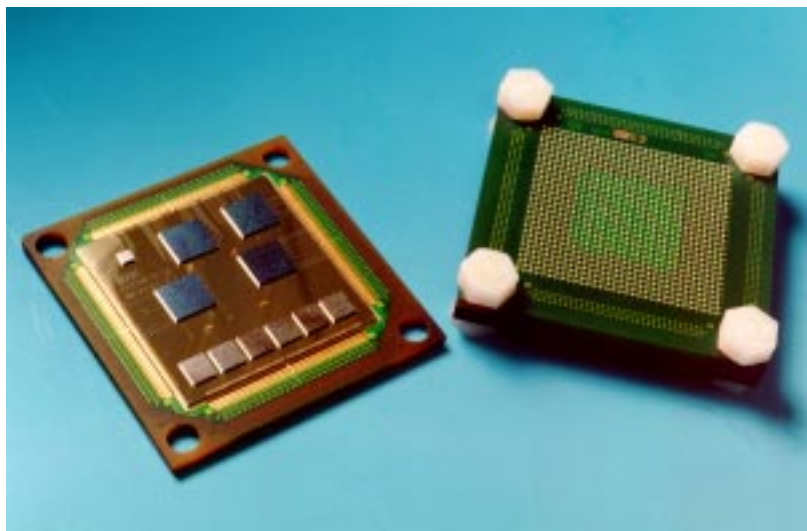


Fig. 11.21: A prototype FERMI MCM in a BGA package.

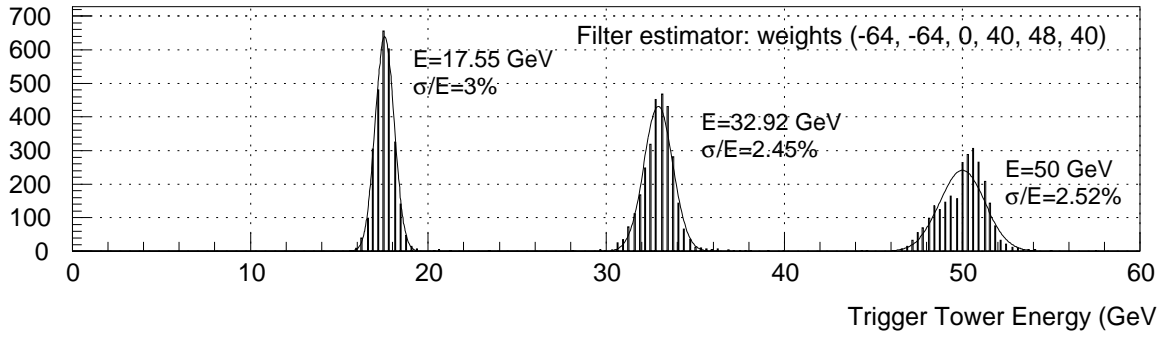


Fig. 11.18: The Trigger energy resolution

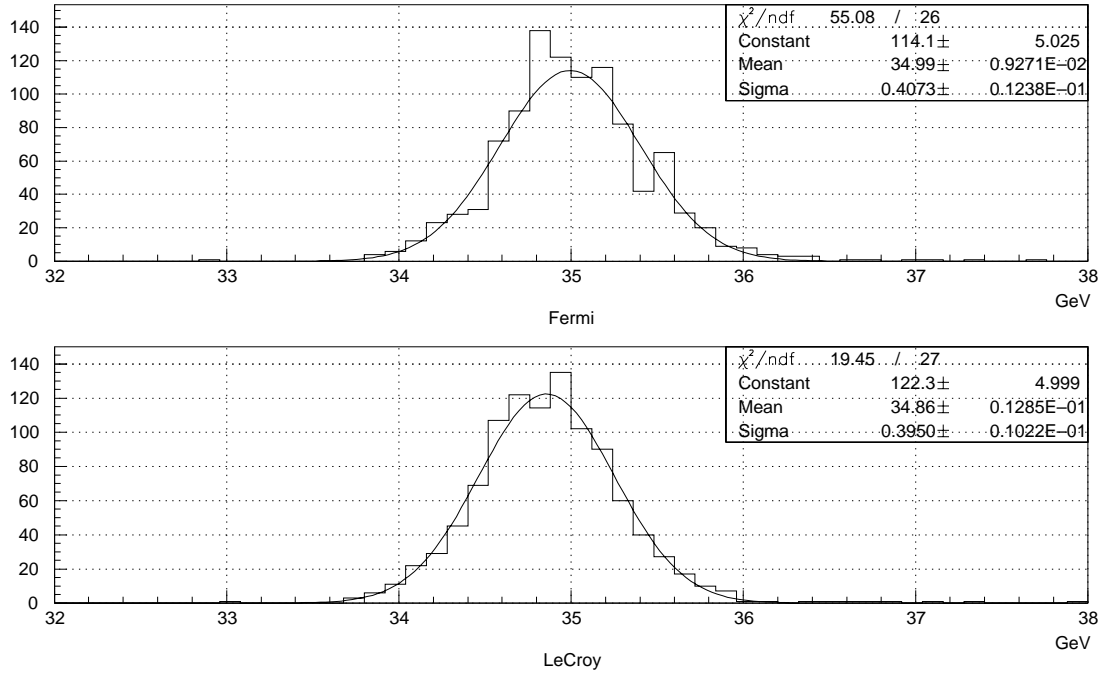


Fig. 11.19: Resolution at 35 GeV with the FERMI readout vs. Charge ADC readout.

11.5 ASSEMBLY AND INSTALLATION

11.5.1 Multichip module

Within the RD16-FERMI project, developments of modern assembly techniques have been one of the goals. As a result, a method of producing MCM-D substrates which can use the flip-chip mounting technique has been evaluated and found very reliable. This assembly method eliminates the classical bond wires for the connection of the individual dies to the substrate which contains all the interconnections. Instead, solder spheres with a diameter of 100 μm , are deposited onto the I/O pads of the dies which are then place upside-down on the substrate and the solder is reflowed, see Fig. 11.20. In this way the MCM becomes an extremely compact and reliable subsystem.

Once the final functionality is determined a mask programmed version will be ordered to improve the reliability of the ASIC.

11.3.7 Data links

There are three types of links within the readout system, the optical connections with the on-detector electronics, see 11.2.3, the copper links between the readout system and the first-level trigger system and the links to the Farm switch.

For the link from the on-detector electronics the environment in the detector forces the use of rad-tolerant implementations while at the counting room end a standard technology can be used. The bandwidth must allow to pass three channels, each with 8 bits of raw data, plus the EDC envelop indicating that a 1.2 Gbit link is required. Severe demands on inter-link synchronisation exist as all samples generated by a particular bunch crossing MUST be retrieved with the same clock edge in the Readout Modules and any loss of sync results in a Fatal error report.

The link to the Trigger will be a 1.2 Gbit serial link using a high-quality copper cable. All links will be of the same length, currently estimated to 20 m, and commercially available serialisers and drivers will be used. Also, the sync requirement is severe for the same reason as above.

For the link to the Farm switch we assume that a common CMS solution will be developed.

11.3.8 Front end driver/detector dependent unit

The FED/DDU module, see Fig. 11.8, is a 9U VME module where the FED part is common to all sub-detectors and the DDU part is tailored to each sub-detector requirements. It contains the necessary interfaces to the VME backplane and to the RDPM which is a dual-port memory where the DDU stores the formatted event blocks for later access by the Farm switch.

For HCAL, and ECAL, the DDU contains the necessary processes to handle the Readout modules. These processes, as understood today, are Data formatting, Calibration and parameter generation and loading as well as in-situ functional tests of the system. The DDU is built around a commercial CPU-DSP chip set and is fully reconfigurable to adapt to the final requirements of the total system.

11.4 PROTOTYPE TEST RESULTS

A set of VME modules were constructed using an analogue dynamic range compressor, a 10-bit ADC, the 3-fold Channel ASIC (see chapter 11.3.1) and the first Filter 1 prototype. These units were, together with the ECAL trigger primitives generator built by Lisbon and Ecole Polytechnique, used to read out a 3x3 ECAL crystal matrix during 1995 test beam period.

Both the trigger information extraction and the detector resolution was tested and Fig. 11.18 and Fig. 11.19 show the results. It should be noted that the compressor was NOT perfectly adapted to the detector and that ONLY 10-bit ADCs were used thus creating a situation where the full performance of the readout system could not be explored.

event conditions (flags) or by external commands. From the insert it can be seen that the coefficient word contains a 10-bit signed FIR coefficient, the corresponding 3-code coefficient and a parity bit.

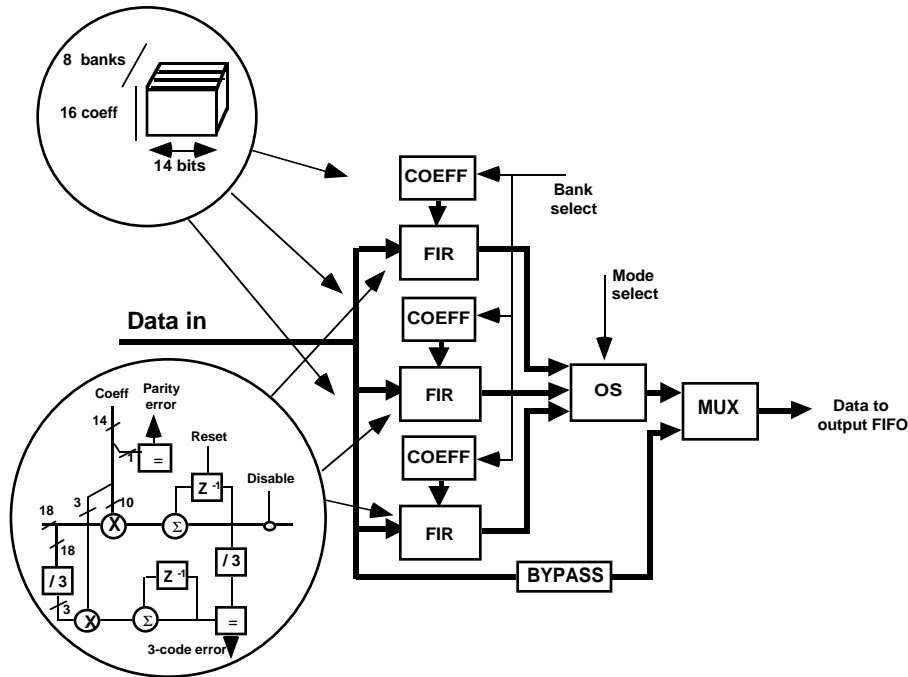


Fig. 11.17: The Filter 2 ASIC

Each FIR is, by its coefficients, optimised for a particular condition, like low signal-to-noise ratio, pile up conditions or, in the case of HCAL to the fluctuations in detector response. The OS operator selects the FIR giving the best result by sorting them according to max. min. or median criteria [2]. This creates a similarity with "loops" or "case" statements in a pattern recognition routine.

Two different error checks are done, parity check on the coefficients and a 3-code check of the filter function, both giving Fatal errors.

Results

The Filter 2 ASIC is being laid out and is expected to come back from foundry in November 1997.

11.3.6 Read out controller ASIC

The Read Out Controller (ROC) will be implemented using a programmable array of the XILINX or ALTERA families. The reason is that the functionality cannot be fully defined at this moment as it is closely related to the central DAQ in particular system design, transfer protocols and error handling.

The functions currently envisaged are, apart from moving data and controlling the Filter 2, to act as the interface between the board wide field bus and the internal control bus, to act as the TAP controller for the MCM wide Boundary scan tests, to gather and transfer to the Board Controller the error bits generated within the MCM and to house the MCM I/O buffers.

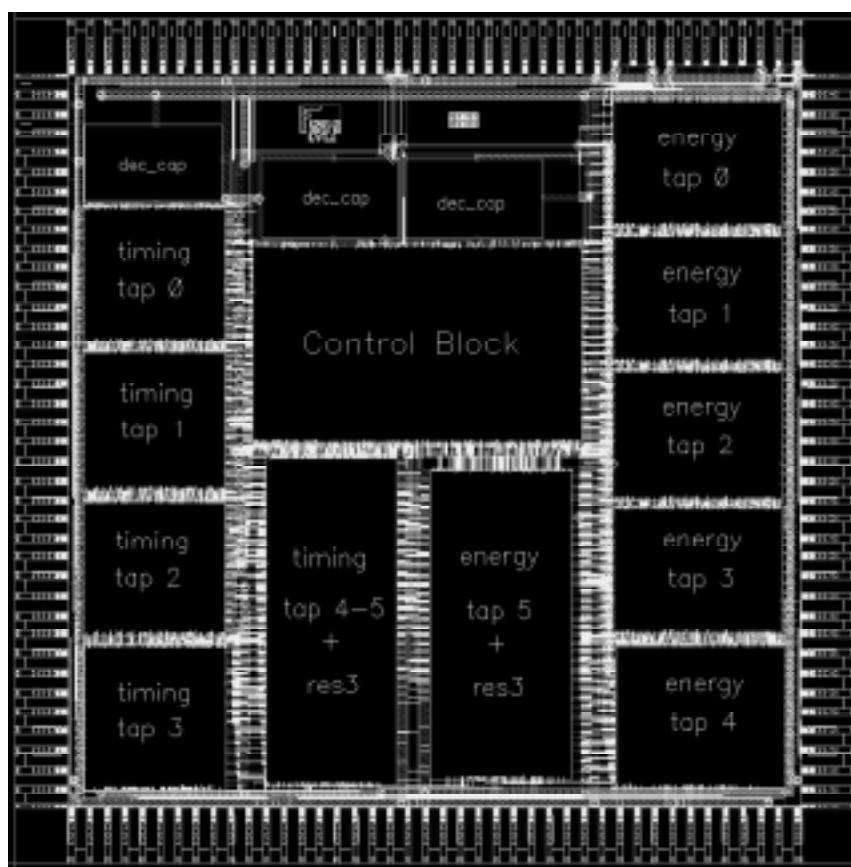
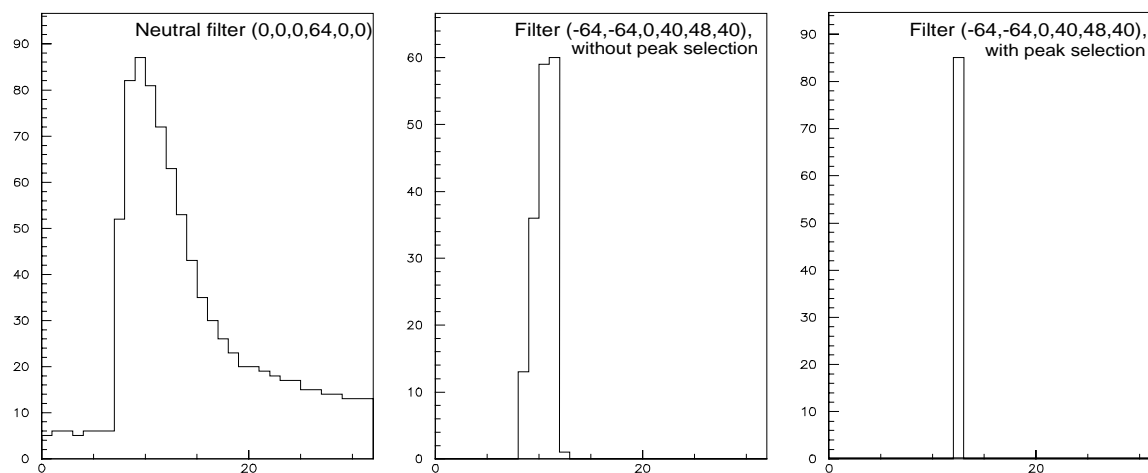


Fig. 11.15: Layout of the Filter 1 ASIC



Three different events taken from the online display

Fig. 11.16: The Filter 1 function

11.3.5 Filter 2 ASIC

Description

The Filter 2 ASIC, see Fig. 11.17, consists of three pipelined FIR taps and an Order Statistics operator supervised by the Read Out Controller. Each FIR filter has an associated coefficient memory consisting of eight banks of 16 locations which can be selected according to

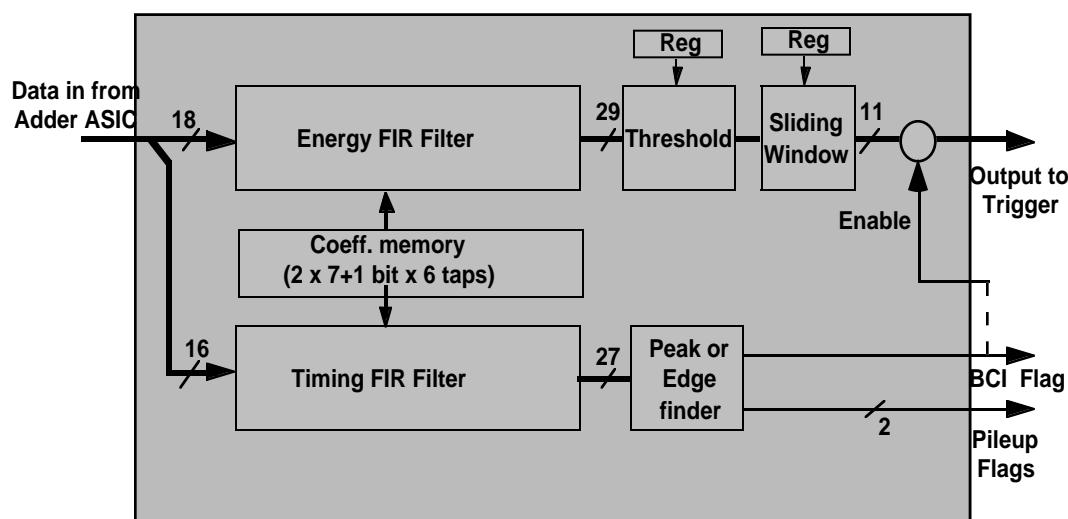


Fig. 11.14: Filter 1 ASIC.

Following the Energy filter is a programmable Threshold and a equally programmable Sliding Window which selects up to 11 bits of the energy. The timing FIR is followed by a Peak or Leading Edge finder that identifies the time origin of the signal, called BCI flag. Also, this circuit detects possible Pile up conditions by checking the number of clocks between two BCI flags and two values can be loaded to define Pile up and Severe Pile up. The corresponding flags are generated for insertion into the Pipe line. The BCI flag is also used to conditioning the energy output in order to produce zero energy except at the correct bunch crossing.

Results

A first version of the Filter 1 ASIC was implemented in the ES2 0.7 μm technology and used extensively in the ECAL H4 beam tests together with the above mentioned Channel ASIC. A second version has been submitted to foundry and is expected to be delivered in August 1997. Fig. 11.15 shows the lay out of the ASIC, while Fig. 11.16 shows some representative test data illustrating possible filter 1 functions.

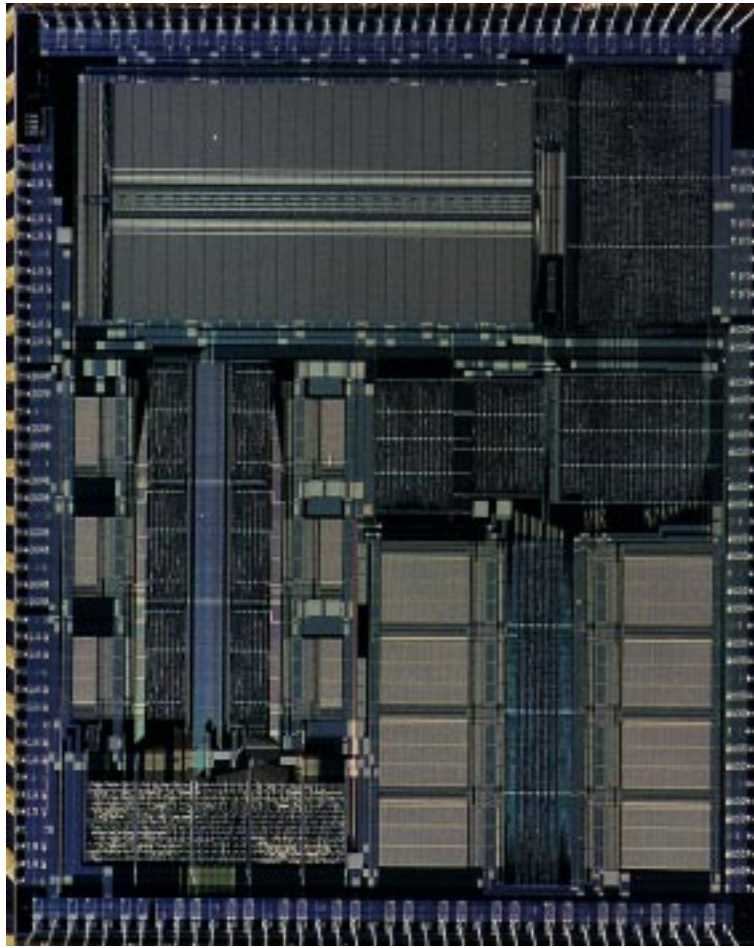


Fig. 11.13: Microphoto of the pipeline ASIC.

11.3.4 Filter 1 ASIC

Description

The Filter 1 ASIC, see Fig. 11.14, consists of two 6-tap FIR filters, one optimised for energy extraction and the other for time (BC) identification. Each tap in the two filters has loadable coefficients with a width of 7 signed bits. The Energy FIR is processing with full resolution in order not to bias the results while the Timing FIR truncates two LSBs. At the input of each filter is a 3-code generator followed by a 3-code filter and, at the output, a 3-code comparison between the results of the filter and its 3-code filter. In case of mismatch a Fatal error is generated. Also, the corresponding 3-code coefficient and a parity bit is added to each tap coefficient, the latter to assure that no transient errors have occurred in the storage.

11.3.3 Pipeline ASIC

Description

The Pipeline ASIC consists of a programmable length Pipeline, built as a rotating buffer, and a set of derandomising buffers. A schematic of the pipeline ASIC appears in Fig. 11.12.

Data from the LUT is combined with the flags from the Filter 1, encoded in a ECC envelope and written into the buffer at each machine clock. The length, i.e. the delay, is programmable between 4 and 256 clocks. A bypass path is built in for test purposes.

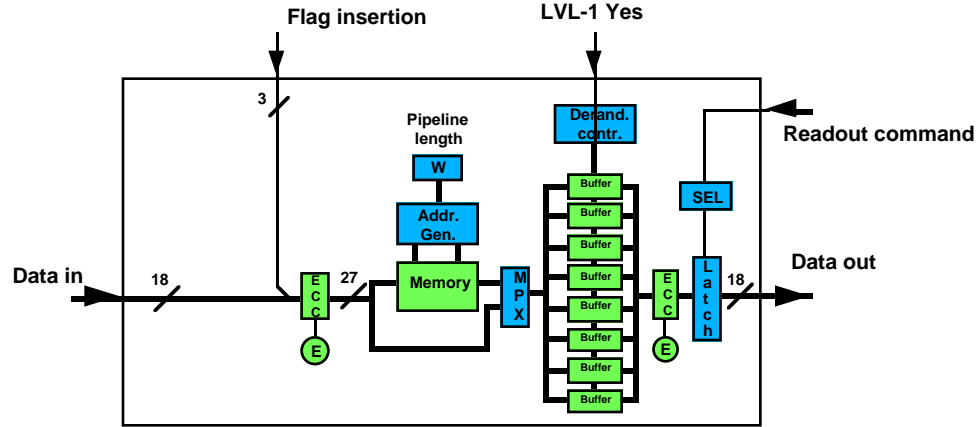


Fig. 11.12: The pipeline ASIC.

At each first-level Yes a time frame, 16 samples long, is written into the next free Derandomising Buffer. If a new Yes arrives within the 16 clocks a new buffer is opened and another time frame is written into it. This creates complete frames for each trigger even in cases of severe pile up.

At the output, the data passes a ECC decoder which will correct any transient bit error occurring within the storage elements. In case of a correction the ECC decoder will issue a Non-Fatal error.

Results

The current version of this ASIC contains the pipeline preceded by a lineariser function which will be disabled in the HCAL application.

A final prototype version, as described above but also including the HCAL lineariser circuit, has been implemented in the AMS 0.8 μm CMOS. The ASIC is currently under test and will be used in the first complete MCM (see chapter 11.4.1). A microphoto of the ASIC is shown in Fig. 11.13.

Each input has a individually programmable "Threshold" function which zeroes data below the loaded value and in case of a data error flagged by the Data Integrity Bit. Also, when the value FFFFF_h is loaded the channel is switched off, i.e. the value is always zero. The adder is protected by a residue 3-code process which generates a Fatal error in case of mismatch between the residue sum and the encoded 3-code of the output value.

Results

The two first versions of the above mentioned Channel ASIC also contained the adder function but to improve flexibility and adaptability the function has been extracted and is now a separate ASIC. The above described version is implemented in AMS 0.8 μm CMOS, and, as can be seen in Fig. 11.11, the surface is not optimised as it was required to use classical wire bonding into PGA packages for the first prototypes. Final version will be adapted to flip-chip bonding thereby eliminating all unnecessary surface.

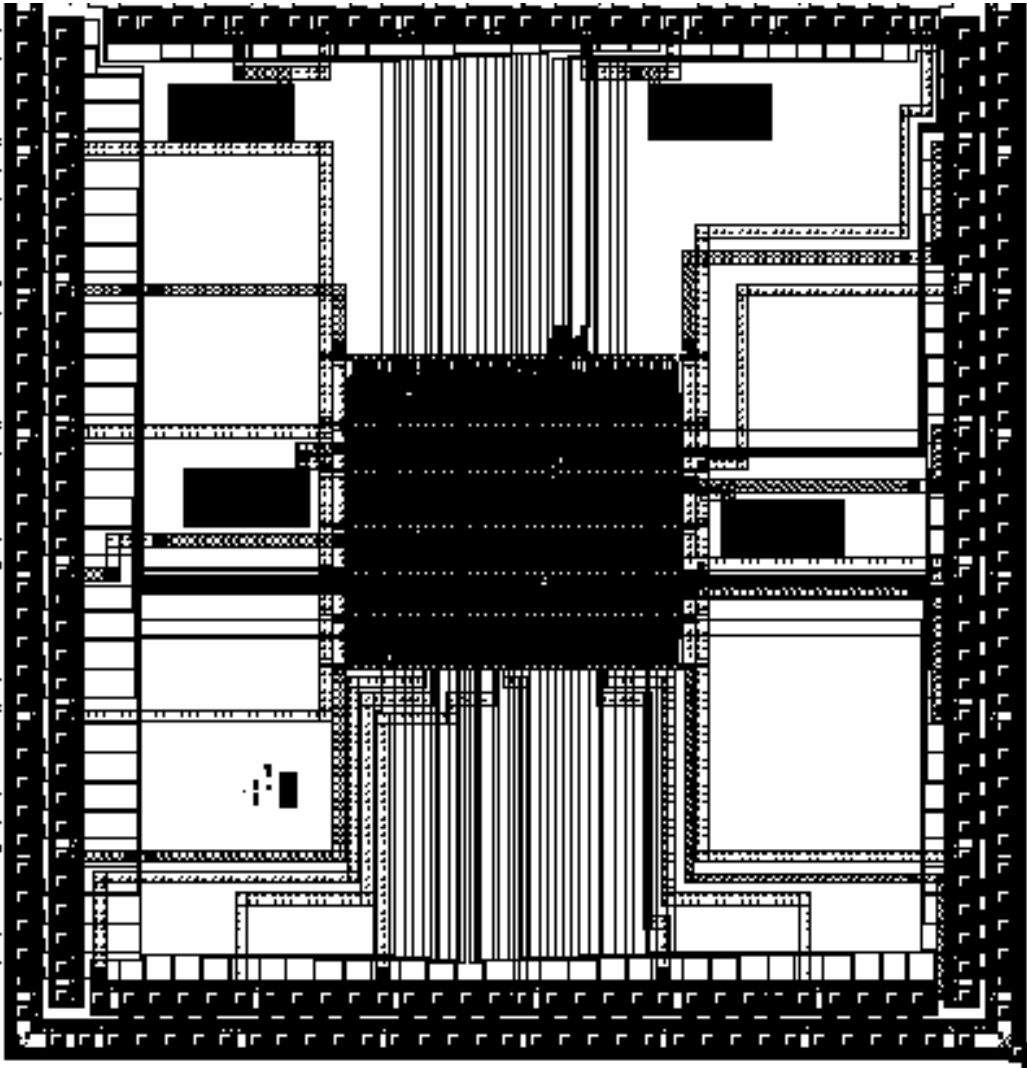


Fig. 11.11: Adder ASIC layout.

A hardwired address parity bit is, for each operation, compared with the calculated parity of the input data which acts as address for the RAM and creates a Fatal error in case of mismatch. The ECC decoder at the output of the ASIC corrects eventual transient faults and generates a Non-Fatal error.

The Data Integrity Bit from the detector to counting room link is passed through a delay to compensate for the memory delay.

Results

This function was an integrated part of the two first versions of the so-called Channel ASIC, and different versions have been produced using different technologies, AMS 1.2 μm , ES2 0.7 μm and AMS 0.8 μm CMOS, starting with a large surface 3-channel ASIC. It contained all the functionality now split between the Lineariser, Adder and Pipeline ASICs.

The second version of the Channel ASIC was extensively used, together with a 10-bit ADC and the original RD16 dynamic range compressor, during the 1996 ECAL H4 beam test runs.

To cope with the difference in requirements between, e.g. ECAL and HCAL, the lineariser is now being implemented as a separate ASIC. Functionally, the HCAL lineariser is identical to the one in the prototype Channel ASIC.

11.3.2 Adder ASIC

Description

The Adder ASIC is a joint ECAL-HCAL development capable of generating trigger sums over 2 to 6 channels. For HCAL, two sums of two channels (HAC1 + HAC2) is generated on the "Partial Sum out" outputs. A block diagram of the adder ASIC is given in Fig. 11.10.

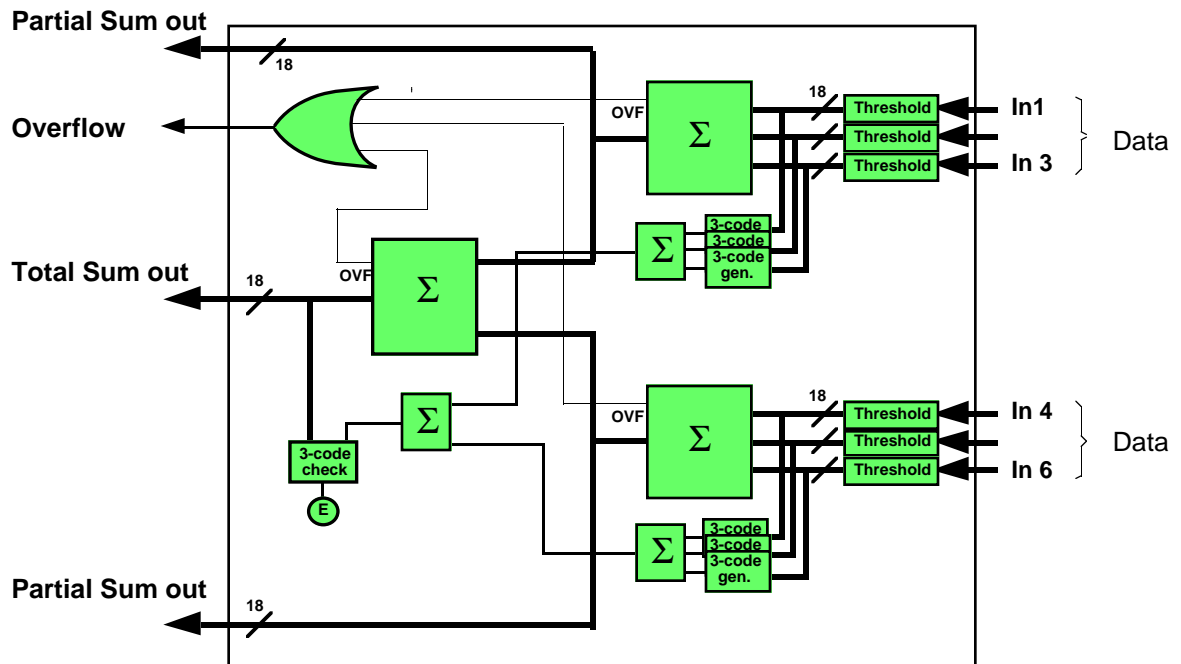


Fig. 11.10: Adder ASIC.

11. TRIGGER AND DATA ACQUISITION ELECTRONICS

channel and their energies. Also, it will be the point where all error information from the downstream system arrive. Actual actions on errors will be specified together with the DAQ group.

The DDU has provisions to execute repeated and standard actions like setting pipeline lengths and loading coefficients and configuration parameters into the Readout Modules. To minimise transfer time the Board Controllers handle, in parallel, the loading of identical parameters to all MCMs.

11.2.8 Testing and diagnostics

All ASICs have the IEEE 1149-1 Boundary Scan circuits implemented with a MCM-wide structure. The Board Controller acts as the local scan controller with a TAP controller on each MCM. Through this function the DDU can request contiguity tests and some functional tests of the system.

A very powerful test is to load the LUTs with simulated data which is sent out at the 40 MHz clock rate into the DAQ and Trigger paths. As the data is known the results can be compared, in real time, with the expected values and a complete diagnosis of all functions can be done under control of the DDU.

Each functional block, links, LUTs, etc. controls its own process and provides one or more error bits of two different classes, Fatal and Non-Fatal errors. Non-Fatal errors, like data being corrected by an Error Correction Code, are histogrammed and an alarm will be given only if the error rate exceeds a predefined level. Fatal errors, like loss of sync in a link, might require the intervention of a higher-level process.

Finally, there are a number of strategically placed "SPY" registers that can be read over the control path at any time to assure proper functioning of a specific block.

11.3 COMPONENTS

11.3.1 Lineariser ASIC

Description

The Lineariser ASIC is built around a 2k x 24 bit RAM whereof 18 bits are available for the data, 5 bits for ECC syndrome bits and 1 bit is the address parity. A multiplexer at the input, together with a counter-latch, allows the downloading of the LUT content over the MCM control bus. A schematic of the lineariser ASIC appears in Fig. 11.9.

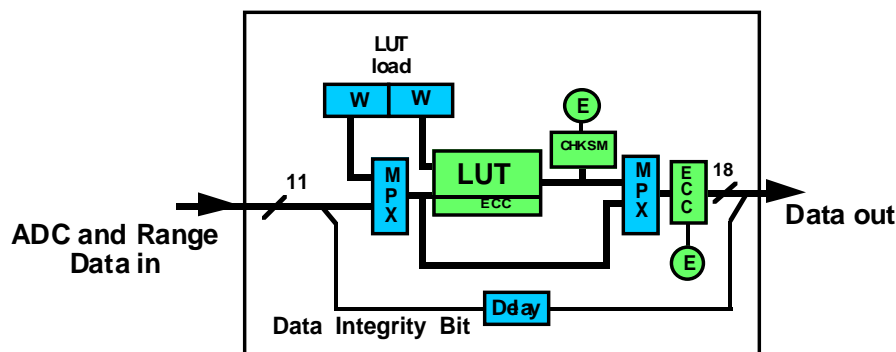


Fig. 11.9: The lineariser ASIC.

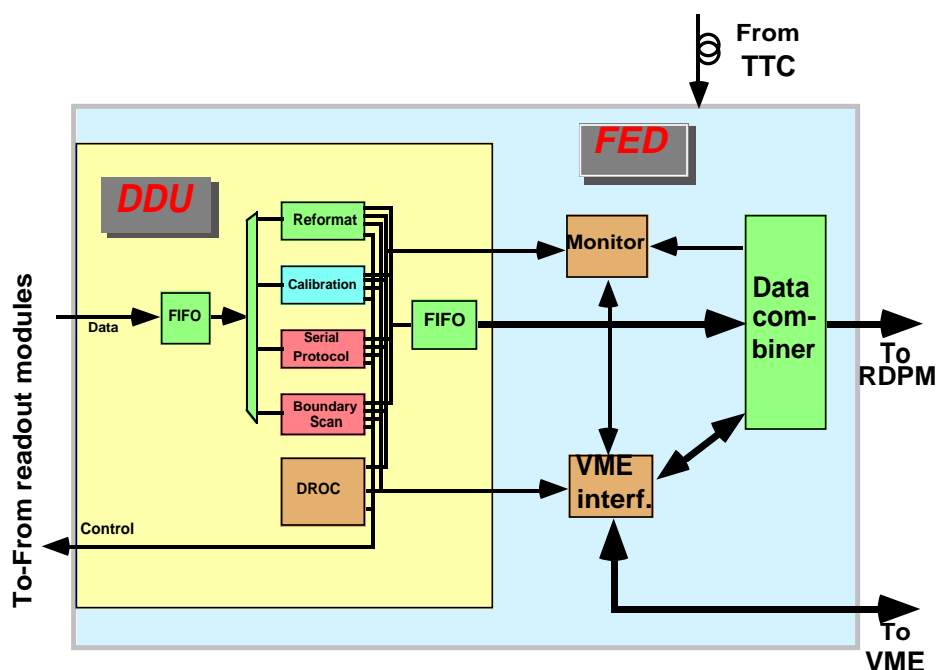


Fig. 11.8: The DDU/FED module.

The detector dependent unit (DDU), which is part of a standardised front end driver (FED) module, controls a set of Readout Modules and performs all required operations on the data, executes hardware functional tests, downloads the required status and coefficient information. It also acts as the interface to the first unit in the central DAQ system, the readout dual port memory (RDPM).

11.2.6 Calibration data

Calibration data is generated either by the laser, the LEDs or the radioactive source. In all three cases, the LUT is programmed for unity transformation. For the pulsed calibration, the front-ends are operated in the normal 40 MHz mode and a properly synchronised first-level trigger accept is sent to the derandomising buffers and the ROC. Here, the filter 2 transformation required is to extract the total signal deposited by a laser or LED pulse.

The source calibration requires readout of many contiguous time frames of sixteen samples each, stored in consecutive derandomiser buffers. First-level trigger accepts occur at a rate determined by processes operating in higher levels of the system. The subsequent Filter 2 operation generates the sum of these time frames (without thresholds) which is then transferred to the RDPM for histogramming in a farm processor.

11.2.7 Control

The control of the entire read out system is supervised by a Local Controller in the VME crate. This will be a commercial CPU which is driving the VME backplane in the crate and also is connected to the LAN Control link system. It will delegate standard operations to the DDU and the Board Controllers, like downloading LUTs, filter coefficients, etc. The Local Controller is responsible for the continuous control of the system behaviour through a "Spy" connection to the Readout Modules. It monitors the data and creates statistics on number of signals per

Integrity Bit and Pile Up flags. As the Pile Up flags are created with a certain latency compared to the samples they will be stored at a location corresponding to the last position of the time frame in the pipeline.

In case of a positive first-level decision the corresponding time frame is transferred to one of the eight Derandomising Buffers together with the bunch crossing number (BCID) from the TTC system and eventual additional status information . At this level a time frame always has the length of 15 samples and the write sequence will be (in Buffer addresses) 1,2,3,4,5,6,.....,15,0 ; which will force the flag, status and BCID information to be stored in the first location of the buffer. At read out the ROC will see, as the first word, the flag information and set the proper working conditions for the Filter 2. In case of overlapping time frames, i.e. Pile Up conditions, a particular sample might be stored in more than one Derandomising Buffer thereby creating, in each buffer, a complete time frame.

The ROC will, for each first-level Yes, extract the information from the Derandomising Buffer corresponding to the event and read a number of samples corresponding to the programmed time frame length. The first word, containing the BCID, flags and Status, is used by the ROC to set up the working conditions for the Filter 2 and as an event data synchronise check. Subsequent words in the time frame are applied both to the filter and to the Output Buffer creating a data block consisting of the individual time frame samples followed by the result of the Filter 2 operation.

Filter 2 consists of three FIR filters combined through a Order Statistics operator (OS). As the samples and the coefficients are applied in sequence a single FIR tap, used in a pipelined mode, is implemented per filter function. The coefficient memory contains eight banks of 16 coefficients, each being a 10-bit signed value. This gives a total of 24 filter combinations and the ROC, with help of the OS operator can, according to flag and status information as well as externally loaded conditions, chose the proper filter for each event. This can be seen as similar to "IF" or "LOOP" statements in an algorithm for optimum pattern recognition.

In the output buffer, event data from the individual channels, together with the Event ID from the TTC system, as well as the corresponding data from the Trigger Primitives pipeline, are merged into a MCM event block. A Board Controller, on the VME module, supervises the transfer of all MCM-blocks to the DDU/FED module, see Fig. 11. 8, where the data is reformatted into one block containing the filtered values tagged with their address and one block with the time frames tagged in the same way. Zero skipping is also performed at this level thus minimising the data volume sent to the DAQ system.

A 1k x 8 bit programmable Look Up table is used to convert the 10-bit linear representation to the required Quad-Linear format which is combined with the corresponding information from another identical trigger tower processing circuit. To this combined information an Error Detection Code (EDC) is added in order to preserve the quality of the information sent to the trigger.

The data with its EDC envelop is serialised and transmitted over a high-quality copper link to the Local Trigger Crate which is placed close to the HCAL electronics.

To cope with the large differences created by the response fluctuations in the detector, two methods have been developed. One is to program the time filter to be edge sensitive, and the other makes use of the total energy sum seen in the timing filter. As both filters are individually programmable in length, the correct energy will coincide with the time tag produced by either method. It has been decided to ignore the true baseline behaviour which, on average, is exponential and simply use the mean of the two presamples as the baseline for the pulse. This means that the two FIR filters use five samples, two for the baseline and three for the pulse information giving another tap free for future implementations.

11.2.5 Second-level trigger data and event data

Requirements

Events accepted by the first-level trigger shall, for the second-level trigger process, generate a single word per channel. The current solution with a non-linear filter consisting of 3 FIR banks and an Order Statistics operator, called Filter 2, fulfills the requirement as the filter algorithm can be controlled by external conditions such as pile up, luminosity and signal amplitude.

Events passing the virtual Second-level trigger shall, per channel, provide the Third-level and subsequent processes with Event Data consisting of a time frame containing the five samples corresponding to the pulse. (See also [4].)

Implementation

The data path (see Fig. 11.3) is common for the second-level- and the event-information as the second-level trigger is a virtual process within the DAQ farm.

The linearised data from the LUT is sent into a pipeline of individually programmable length (4 to 256 locations) where the data is stored during the first-level latency. Each positive decision by the first-level process initiates a transfer of a time frame of programmable length (max. 16) to one of eight derandomising buffers. If a second Level-1-Yes arrives during the transfer of a time frame a second derandomiser is opened and the overlapping data is written to the two destinations thus creating individual time frames even in cases of severe pile up. A Read Out Controller (ROC) within the MCM supervises the extraction of the data and the processing by the Filter 2. For each channel the ROC extracts both the individual time frame values and the result of the Filter 2 operation where the Filter 2 value will be used by the virtual second-level trigger and the time frame by the subsequent processes. Formatting of the event block is done in the DDU (see 11.3.6). This formatting creates one block for the second-level trigger, containing only the filter values, and one block for the third-level and data storage containing the time frames.

The pipeline is based on a dual-port RAM and implemented as a rotating buffer of programmable length. It contains the data samples and corresponding information i.e. Data

Implementation

Linearised data from the outputs of the LUTs are applied to individual and programmable threshold functions. These functions suppress data below the programmed values as well as providing zero output data if either the loaded value is FFFF_h (switch off the channel) or if the Data Integrity Bit indicates that the information has been corrupted at a preceding stage.

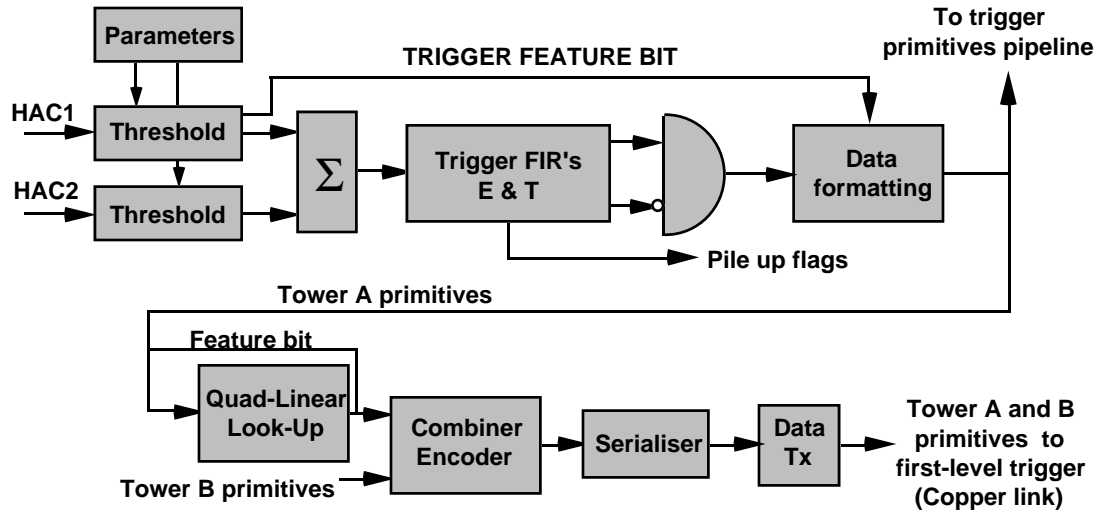


Fig. 11.7: First-level trigger feature extraction.

Within the threshold circuit a Feature Bit is generated as a function of the relation between the energy depositions in HAC1 and HAC2. The simplest implementation is to set the bit when the HAC1 energy is above a specified value.

The thresholded data from HAC1 and the corresponding HAC2 compartments are added to form a Trigger Tower sum. This addition is performed with full 16-bit precision in order to avoid truncation errors. Also, the adder function is protected by a 3-code residue coding to assure the quality of the operation.

The tower sum is applied to two 6-tap finite impulse response (FIR) filters, one optimised for the energy extraction and one for the time identification. These filter functions are using data with full 16-bit resolution and 7-bit signed coefficients. Both the coefficients and the length of the filters are programmable. The Time Flag conditions the energy information giving an output value of zero except at the bunch crossing that corresponds to the origin of the information. Both filters are protected by 3-code residue coding to assure the quality of the results. Also, flag bits, called pile up flags, are generated by the timing filter to tag events where the distance in time is below a programmed minimum value. Two such flags are generated, one for severe pile up and one for light pile up. The definition of light and severe is done by programming the number of bunch crossings required for each case.

Thereafter, a sliding window with a width of 10 bits is applied in order to truncate the data to the required range of 500 MeV to 500 GeV and the above mentioned Feature Bit is included at the output. The place of the window is programmable.

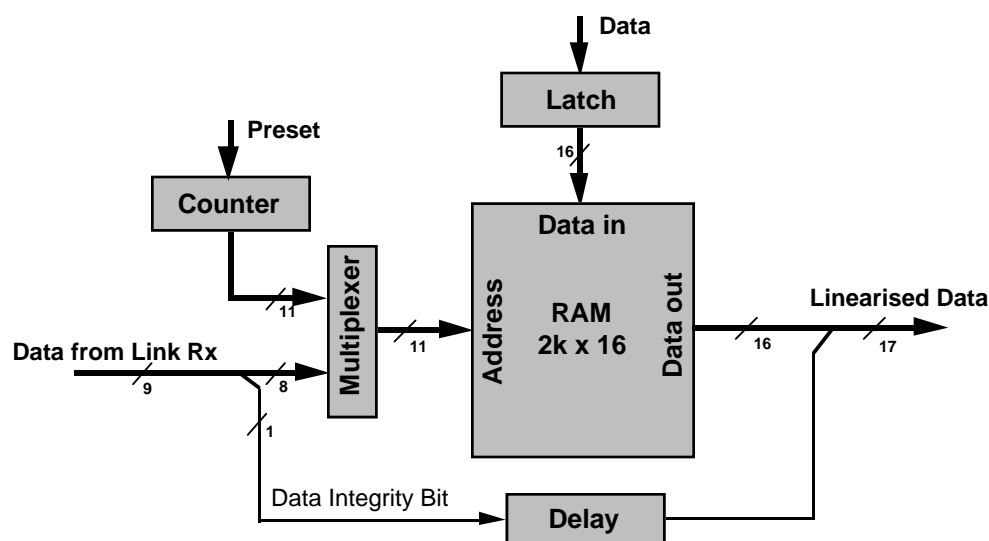


Fig. 11.6: The look-up table.

Once the behaviour of the detector and the QIE-ADC combination is known and the LUT has been loaded with the proper correction constants, the data used for subsequent processes are absolute i.e. no correction constants are required at any stage. However, as the LUT content is known the original data can be restored at any moment during both the on-line and off-line analysis.

In order to preserve synchronism the Data Integrity Bit is routed around the LUT and through a delay corresponding to the access time of the LUT.

11.2.4 First-level trigger data

Requirements

The HCAL first-level trigger information, as seen by the trigger [3], shall have a programmable quad-linear format with a width of 8 bits per tower. This solution was chosen to allow the tailoring of the energy response in order to be able to send information both on very low energy depositions like muons as well as having a reasonable resolution over the required range. This range is set to 500 MeV - 500 GeV.

A Feature Bit has been included to indicate high energy deposition in HAC1 in order to help resolve problems induced by the dead zone between ECAL and HCAL and improve pion-electron separation.

Two towers should be sent over one serial connection.

Data, that has been corrupted either by the link or any other function ahead of the trigger feature extraction, should be set to zero.

Special care must be taken to extract the correct energy and time taking into account the statistical fluctuations of the detector response. A schematic of the feature extraction is shown in Fig. 11.7.

The Board Controller, see Fig. 11.4, organises the transfer of all information belonging to a particular event from the derandomisers of the individual channels in the MCMs to the DDU. In the DDU the information is formatted according to the requirements of the subsequent stages in the DAQ chain.

11.2.2 Data Links between detector and counting room

On the detector the compressing and digitising front ends are combined three-by-three and applied to the input serialiser of the optical link. This combined information is transported over a single fibre at a rate of 1.2 Gbit/s. At the other end, in the Counting Room, the link receiver will demultiplex the data, retrieve the clock, synchronise the data to the local phase of the 40 MHz acquisition clock and perform a Data Integrity Check, see Fig. 11.5. The Data Integrity Bit accompanies the sample(s) throughout the system and is used to, in the trigger path, to zero the data at the level of the threshold function (see below) and will be read out together with the associated data by the DAQ system for later use.

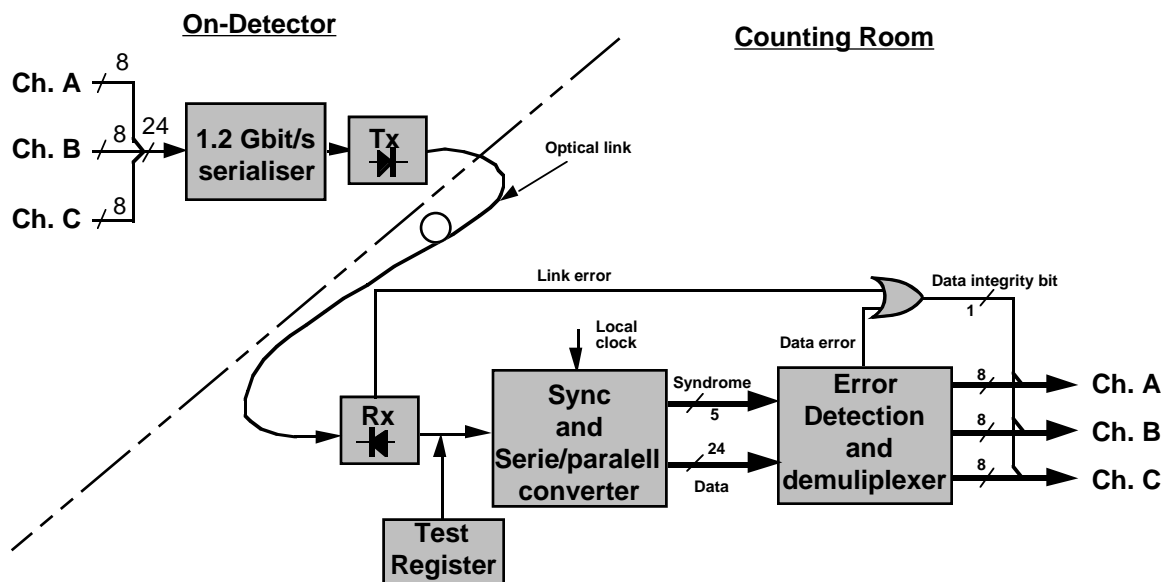


Fig. 11.5: Front end optical links.

11.2.3 Linearisation of the data

The data arriving from the Front End link receiver circuit is applied to a Look Up Table while the Data Integrity Bit is passed around with the appropriate delay. Despite that the data requires only 256 locations (8 bits) a 2 kWord x 17 bit LUT is being used. The LUT is serving two different purposes, linearise and restore the full dynamic range of the acquired data and, for test purposes, being a programmable source of 2048 consecutive samples allowing a full test of all feature extracting functions and readout procedures. Fig. 11.6 shows the functional diagram of the LUT.

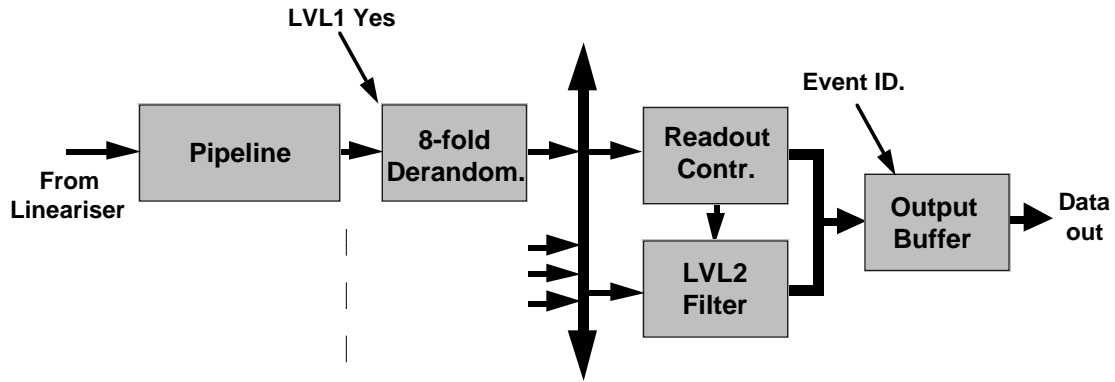


Fig. 11.3: Functional diagram of the DAQ path.

11.2 ARCHITECTURE AND FUNCTIONALITY

11.2.1 System layout

The HCAL readout system is divided into two main parts, the on-detector electronics and the off-detector electronics. The first part consists of the Hybrid Photo Detector, the QIE compressing function with eight ranges, 5 bit ADC and a Control ASIC per channel and the latter consists of the feature extraction and storage elements which will be discussed in detail below (see Fig. 11.4).

Each on-detector channel produces 8 (5+3) bits of information at every Bunch Crossing clock and this allows three channels to be multiplexed onto one high-speed optical link. These links arrive in the counting room where the data is demultiplexed and routed to the digital part of the readout system.

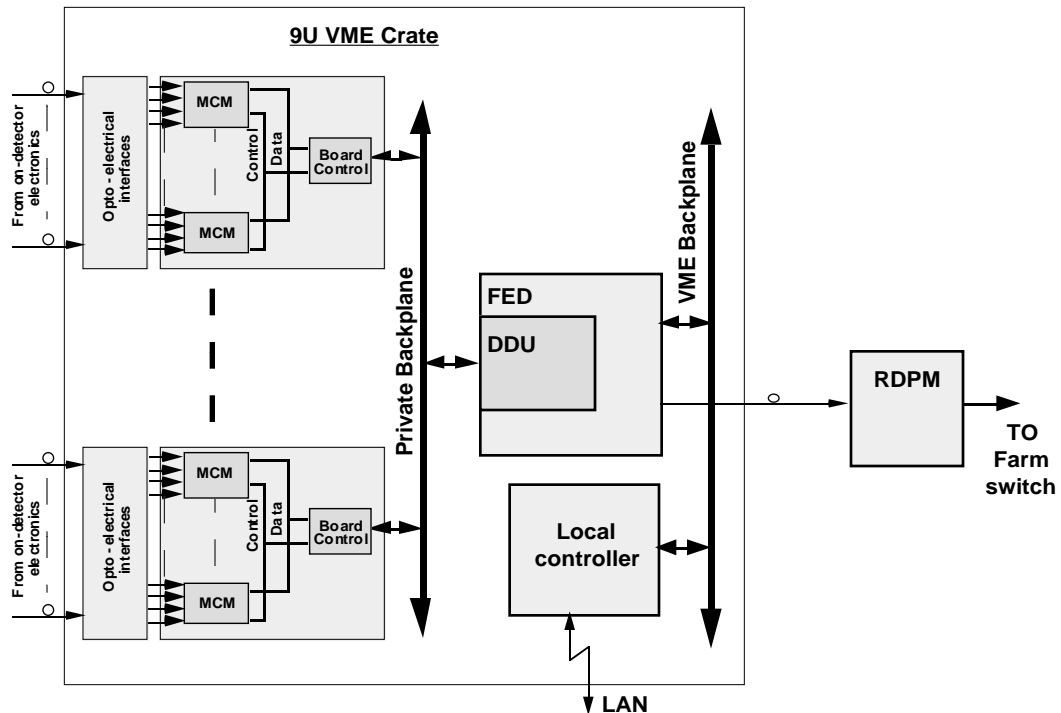


Fig. 11.4: Overview of the digital part of the readout system.

corresponding data from the individual channels. Fig. 11.2 shows the main functions of the trigger primitive extraction circuit.

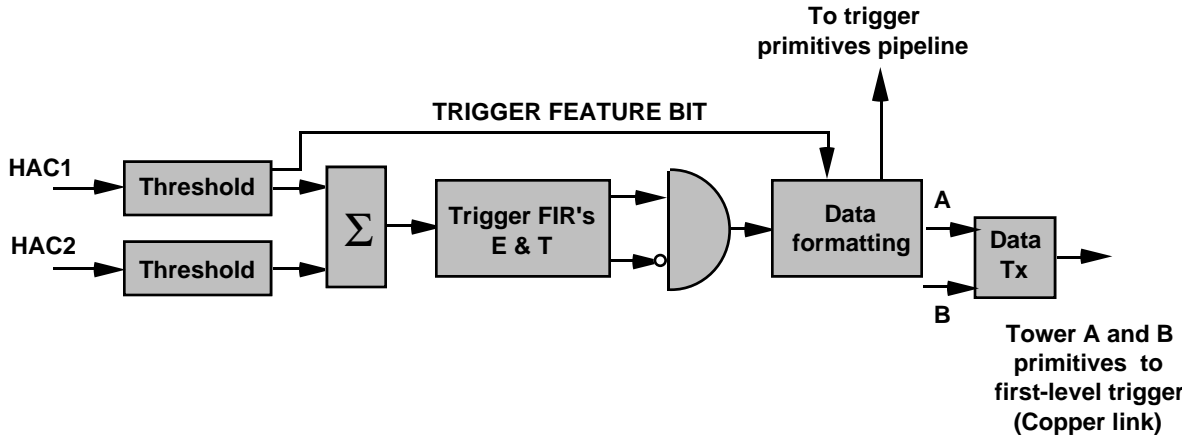


Fig. 11.2: Functional diagram of the trigger path.

11.1.3 Data acquisition system

The expanded and linearised channel data and the corresponding trigger primitives are stored in pipelines consisting of individual dual-port memories implemented as circular buffers with individually programmable length (4 to 256 positions). A temporal environment, a time frame of programmable length (max. 16), is associated with each event accepted by the first-level trigger. These time frames are, upon a positive first-level decisions, transferred into a set of derandomisers for later processing and readout.

The Readout controller supervises the extraction of data, from the derandomisers, either in the form of complete time frames or as digitally filtered values of the energy. In the latter case the information contained in a time frame is extracted using an adaptive non-linear digital filtering techniques optimised for extracting a precise value of the energy even in the presence of noise and jitter. It is envisaged that the filtered readout should be default when pushing data to the virtual second-level trigger process. This process could, however, return for selective readout of full time frames, which might be necessary in order to resolve specific conditions. Currently, it is envisaged to transmit full time frames to the third-level trigger and subsequent off-line analysis.

It should be noted that, as the linearisation constants are known, the off-line analysis can, at any moment, retrieve the raw data generated by the front end digitiser electronics.

Fig. 11.3 shows the functional diagram of the DAQ path.

11. TRIGGER AND DATA ACQUISITION ELECTRONICS

11.1 INTRODUCTION

11.1.1 Overview

Digitised results arriving from the on-detector electronics on optical fibre links are converted to electrical signals and applied, channel by channel, to the readout system. The first step in the process is to linearise the data by means of a Look-Up Table (LUT) containing the inverse function of the QIE compression and the detector response. This linearised data provides the first-level trigger with time and energy information per trigger tower and is also stored in a pipeline for later readout according to the first-level trigger decision. Fig. 11.1 shows a simplified block diagram of the chain. The implementation is making full use of modern assembly techniques e.g. Multi-Chip-Modules (MCM) and Chip-on-Board technologies. Also, fault tolerance and error detection architectures are used throughout the system thus creating a highly reliable system. The HCAL readout electronics is based on the developments done within the RD16-FERMI project [1,2].

All electronics in the counting room are implemented as 9U VME modules making use of the rear transition card for interfacing purposes. A Detector Dependent Unit (DDU), being part of the Front End Driver (FED), supervises the read out of a VME crate or part thereof. A total of 14 memory modules (RDPMs) are envisaged for the HCAL at the entry of the Farm switch.

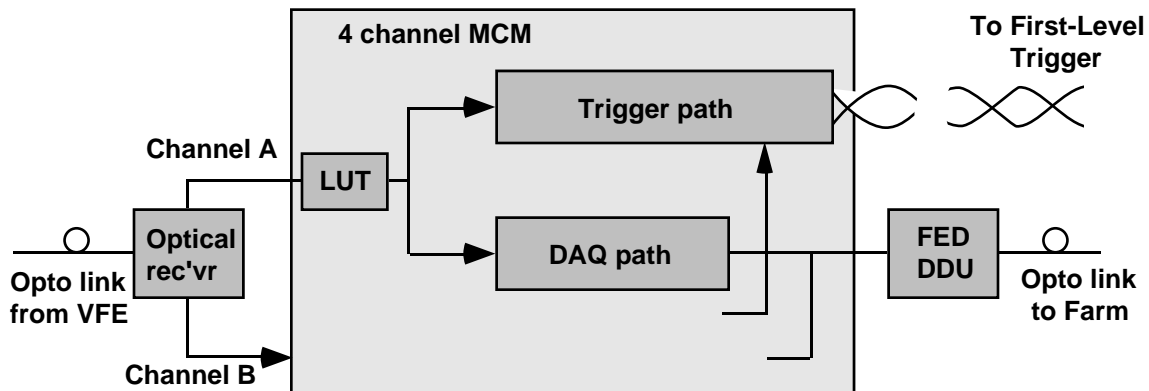


Fig. 11.1: Simplified block diagram of the HCAL readout system

11.1.2 First-level trigger system

The linearised data is taken, immediately after the LUT, through individual thresholding circuits and applied to an adder circuit where the information from HAC1 and the corresponding HAC2 are combined to form a trigger tower. This data is applied to a dual FIR filter circuit which extracts the energy and Bunch Crossing information and formats the data according to the trigger system requirements (trigger primitives). Also, a Trigger Feature Bit is generated as a function of the energy relation between HAC1 and HAC2 and included into the trigger primitives.

The information from two trigger towers is multiplexed onto one high-speed copper link and transferred to the first-level trigger system. In parallel, the individual primitives are stored in pipeline circuits of programmable length for subsequent readout together with the